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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,778	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030480US1	6264

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/675,778	DEWITT ET AL.	
	Examiner	Art Unit	
	Dillon J. Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/9,30, 2/14, 5/8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are pending.

Papers Filed

2. Examiner acknowledges receipt of amended claims, amended specification, and information disclosure statement all filed 8 May 2006; information disclosure statements filed 14 February 2006, 30 January 2006 and 9 January 2006.

New Rejections

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Davidson et al. (U.S. Patent No. 6,446,029) hereinafter referred to as Davidson.

5. As per claim 1, Davidson discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction (Col. 7 line 64 - Col. 8 line 32), wherein a threshold value is located in the indicator (Fig. 5B threshold registers 521-525); and counting executions

of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value (Col. 8 lines 61-65). *The examiner asserts that, as described in col. 7 line 64 – col. 8 line 32, the instruction tag and the threshold value registers collectively comprise the "indicator". As such, the indicator contains the threshold values.*

6. As per claim 2, Davidson discloses the method of claim 1, wherein the counting step comprises:

determining whether the time to execute the instruction exceeds the threshold value; (Col. 8 lines 61-65)

generating, by an instruction cache, a signal indicating that executions of the instruction are to be counted if a determination is made that the time for executing the instruction exceeds the threshold value; (tagged instructions, col. 7 line 64 – col. 8 line 32) *The examiner asserts that logic block generating the tag constitutes a portion of the instruction cache as at least one instruction is temporarily held there before executing.*

receiving the signal generated by the instruction cache at a performance monitor unit; and incrementing a counter in the performance monitor unit each time the instruction is executed in response to receiving the signal from the instruction cache. (Col. 5 line 38-40)

7. As per claim 4, Davidson discloses the method of claim 1, wherein the indicator is located in a shadow memory. *The examiner asserts that the tag resides in memory.*

If it did not, the processor would have no way to know which instructions are to be monitored and which are not.

8. As per claim 5, Davidson discloses the method of claim 1, wherein the instruction is received in a bundle and wherein the indicator comprises at least one spare bit in a field in the bundle. *The examiner asserts that the processor is capable of executing multiple instructions per clock cycle (Col. 5 lines 1-2), further, a bundle may only encompass a single instruction. The examiner asserts that as soon as an instruction is tagged (col. 7 line 64 – col. 8 line 32), the tag is encompassed in the instruction bundle.*

9. As per claim 6, Davidson discloses the method of claim 1, wherein the counting step comprises:

determining whether the time to execute the instruction exceeds the threshold value; (Col. 8 lines 59-65)

generating, by an instruction cache, a signal indicating an interrupt is present if a determination is made that the time for executing the instruction exceeds the threshold value; *Examiner asserts that thresholder 520 generates a signal indicating a count should occur.* (Col. 8 lines 59-65)

receiving the signal generated by the instruction cache at an interrupt unit; and executing code, by the interrupt unit, to count each execution of the instruction. (Col. 8 lines 59-66)

10. As per claim 7, Davidson discloses the method of claim 6, wherein the code also gathers information from a call stack (Fig. 6A completion table 600) for the instruction. (Col. 9 lines 25-33) *Threshold values 605 are transferred to the threshold registers and used in determining whether to count or not.*

11. As per claim 8, Davidson discloses the method of claim 1, wherein the threshold is a number of clock cycles. *Inherently, the interval values stored in threshold registers must be multiples of clock cycles as a processor uses a clock to determine all timing requirements.*

12. As per claim 9, Davidson discloses a method in a data processing system for processing instructions, the method comprising: receiving an initial instruction at a processor in the data processing system, wherein the initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction; and counting executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value. (Col. 11 lines 17-20) *The examiner asserts that in order to load/store a threshold value directly to the thresholder, a first instruction must occur, as the processor cannot operate without an instruction to tell it what to do. That load/store instruction must inherently contain the threshold value to be compared to.*

13. As per claim 10, Davidson discloses the method of claim 9, wherein the counting step comprises:

determining whether the time to execute the subsequent instruction exceeds the threshold value; (Col. 8 lines 59-65)

generating, by an instruction cache, a signal indicating that each execution of the subsequent instruction is to be counted if a determination is made that the time for executing the subsequent instruction exceeds the threshold value; (Col. 8 lines 59-65)

receiving the signal generated by the instruction cache at a performance monitor unit; and incrementing a counter in the performance monitor unit each time the subsequent instruction is executed in response to receiving the signal from the instruction cache. (Col. 8 lines 59-66)

14. As per claim 11, Davidson discloses a method in a data processing system for processing data, the method comprising: responsive to a request to access data, determining whether an indicator is associated with the data (Col. 7 line 64 - Col. 8 line 32), wherein a threshold value is located in the indicator (Fig. 5B threshold registers 521-525); and counting access to the data if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value. (Col. 8 lines 61-65) *The examiner asserts that a load/store instruction has an indicator associated with it and the instruction is associated with the data it is accessing, therefore the indicator is also associated with the data. When the instruction in question is a load/store instruction (Col. 6 lines 12-14) comparing the threshold for execute stage will tell if the*

load/store was accomplished in a time greater than the threshold value. The examiner asserts that, as described in col. 7 line 64 – col. 8 line 32, the instruction tag and the threshold value registers collectively comprise the "indicator". As such, the indicator contains the threshold values.

15. As per claim 12, Davidson discloses the method of claim 11, wherein the counting step comprises: generating an exception if the indicator is associated with the data and if the time to access the data exceeds the threshold value. *The examiner asserts that a signal is generated by the thresholder upon detection* (Col. 8 lines 59-65)

16. As per claim 13, Davidson discloses the method of claim 11, wherein the counting step comprises:

determining whether the time to access the data exceeds the threshold value; (Col. 8 lines 59-65)

generating, by a data cache, a signal indicating that accesses of the data are to be counted if a determination is made that the time for accessing the data exceeds the threshold value; (Col. 8 lines 59-65) *The examiner asserts that thresholder constitutes a data cache, as data is temporarily stored therein.*

receiving the signal generated by the data cache at a performance monitor unit; and incrementing a counter in the performance monitor unit each time the data is accessed in response to receiving the signal from the data cache. (Col. 8 lines 59-66)

17. As per claim 14, Davidson discloses the method of claim 11, wherein the counting step comprises:

determining whether the time to access the data exceeds the threshold value; (Col. 8 lines 59-65)

generating, by a data cache, a signal indicating an interrupt is present if a determination is made that the time for accessing the data exceeds the threshold value; (Col. 8 lines 59-65) *The examiner asserts that thresholder constitutes a data cache, as data is temporarily stored therein. Further, the signal generated by the thresholder constitutes an interrupt.*

receiving the signal generated by the data cache at an interrupt unit; and executing code, by the interrupt unit, to count accesses of the data. (Col. 8 lines 59-65)

18. As per claim 15, Davidson discloses the method of claim 11, wherein the data is located in a memory location. *The examiner asserts the data being accessed in a load or store is located in a memory location.*

19. As per claim 16, Davidson has taught a processing system performing the method of claim 1, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 1 above.

20. As per claim 17, Davidson has taught a processing system performing the method of claim 2, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 2 above.

21. As per claim 18, Davidson has taught a processing system performing the method of claim 6, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 6 above.

22. As per claim 19, Davidson has taught a processing system performing the method of claim 9, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 9 above.

23. As per claim 20, Davidson has taught a processing system performing the method of claim 10, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 10 above.

24. As per claim 21, Davidson has taught a processing system performing the method of claim 11, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 11 above.

25. As per claim 22, Davidson has taught a processing system performing the method of claim 12, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 12 above.

26. As per claim 23, Davidson has taught a computer program product in a computer readable medium (Col. 12 line 62 – Col. 13 line 6) performing the method of claim 1, consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 1 above.

27. As per claim 24, Davidson has taught a computer program product in a computer readable medium (Col. 12 line 62 – Col. 13 line 6) performing the method of claim 9, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 9 above.

28. As per claim 25, Davidson has taught a computer program product in a computer readable medium (Col. 12 line 62 – Col. 13 line 6) performing the method of claim 11, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 11 above.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davidson.

31. As per claim 3, Davidson discloses the method of claim 1, wherein the threshold value is stored in the indicator but fails to disclose wherein the threshold value is a three-bit value.

32. Using three bits to represent the threshold value would be beneficial in that a small amount of logic is needed to represent the value and up to eight different values can be produced.

33. It would have been obvious to one of ordinary skill in the art at the time of invention to have included three bits in the representation of the threshold values for the benefit of allowing eight different values with a small amount of logic. Further, as shown in In re Rose, 105 USPQ 237 (CCPA 1955) changes in size/range are generally not given patentable weight or would have been obvious improvements.

Response to Arguments

34. Prior objections to pages 1 and 2 of the specification and claims 1, 9 , 14, 19 and 24 have been withdrawn in favor of amendments filed 8 May 2006.

35. Prior rejection of claims 23-25 under 35 USC 101 is withdrawn in favor of amendments filed 8 May 2006.

36. Objection to the title stands. The examiner suggests: "Method and apparatus for counting data accesses and instruction executions that exceed an execution time threshold"

37. Applicant's arguments filed on 8 May 2006 have been fully considered but they are not persuasive.

38. Applicant argues the novelty/rejection of claim 1 on pages 10-11 of the remarks, in substance that:

"The threshold values are clearly not located in an indicator associated with an instruction as required by amended claim 1."

39. These arguments are not found persuasive for the following reasons:

a. The examiner asserts that the term "indicator" has not been expressly defined in either the claims or specification and, hence, has been awarded its broadest reasonable definition. As such, both the bits marking the instructions to be tracked and the registers storing the threshold values in Davidson's processor comprise the "indicator" claimed by Applicant.

Conclusion

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

41. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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